FIG. 1

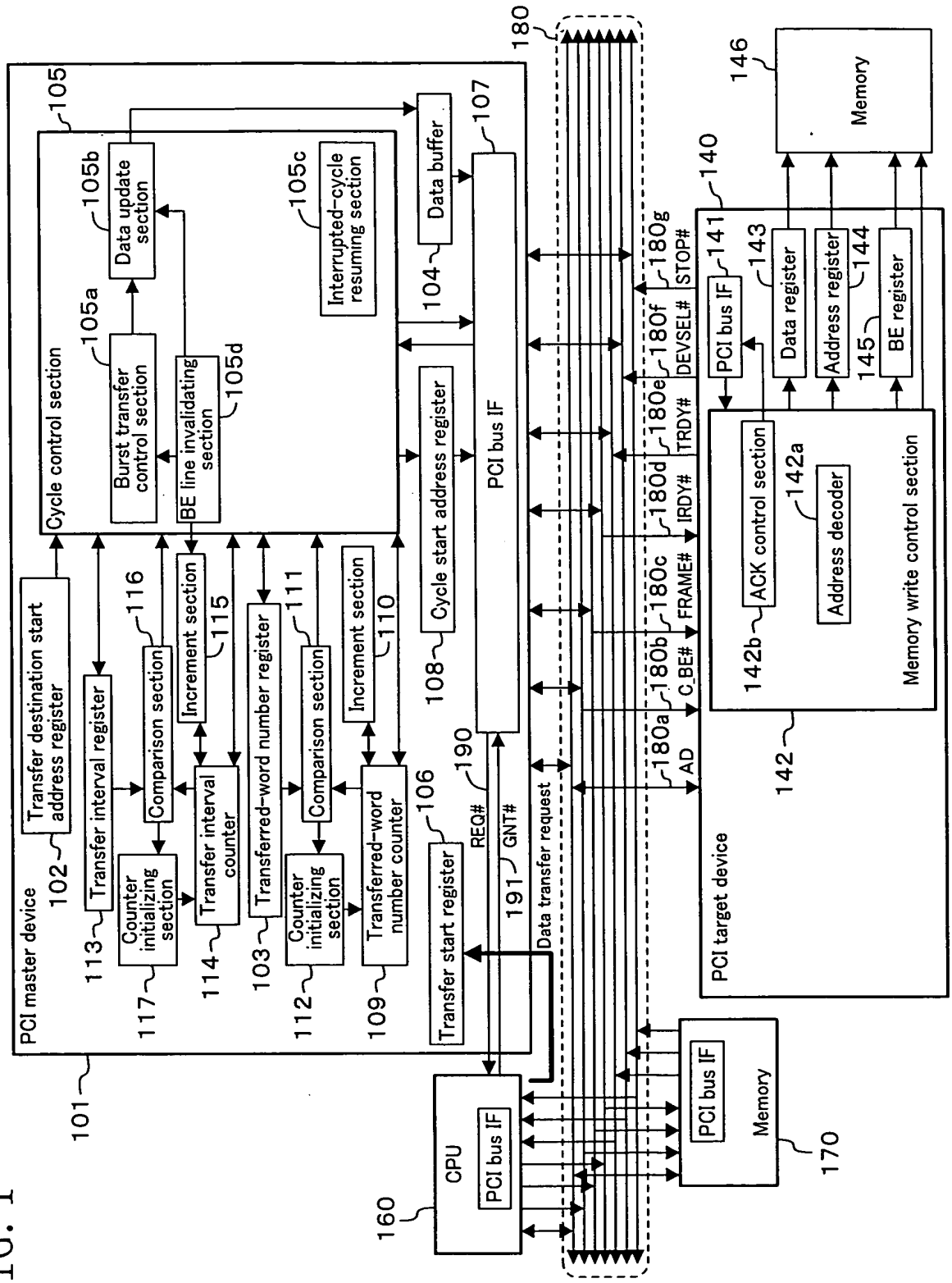

PCI master device
101
Cycle control section
105
Transfer destination start address register
102
Transfer interval register
113
Counter initializing section
117
Comparison section
116
Transfer interval counter
114
Increment section
115
Transferred-word number register
103
Counter initializing section
112
Comparison section
111
Transferred-word number counter
109
Increment section
110
Transfer start register
106
Burst transfer control section
105a
Data update section
105b
BE line invalidating section
105d
Interrupted-cycle resuming section
105c
Data buffer
107
Cycle start address register
108
PCI bus IF
104
180
REQ#
190
GNT#
191
Data transfer request
CPU
160
PCI bus IF
Memory
170
AD
180a
C_BE#
180b
FRAME#
180c
IRDY#
180d
TRDY#
180e
DEVSEL#
180f
STOP#
180g
PCI target device
142
Memory write control section
ACK control section
142b
Address decoder
142a
PCI bus IF
141
140
Data register
143
Address register
144
BE register
145
Memory
146

FIG. 2

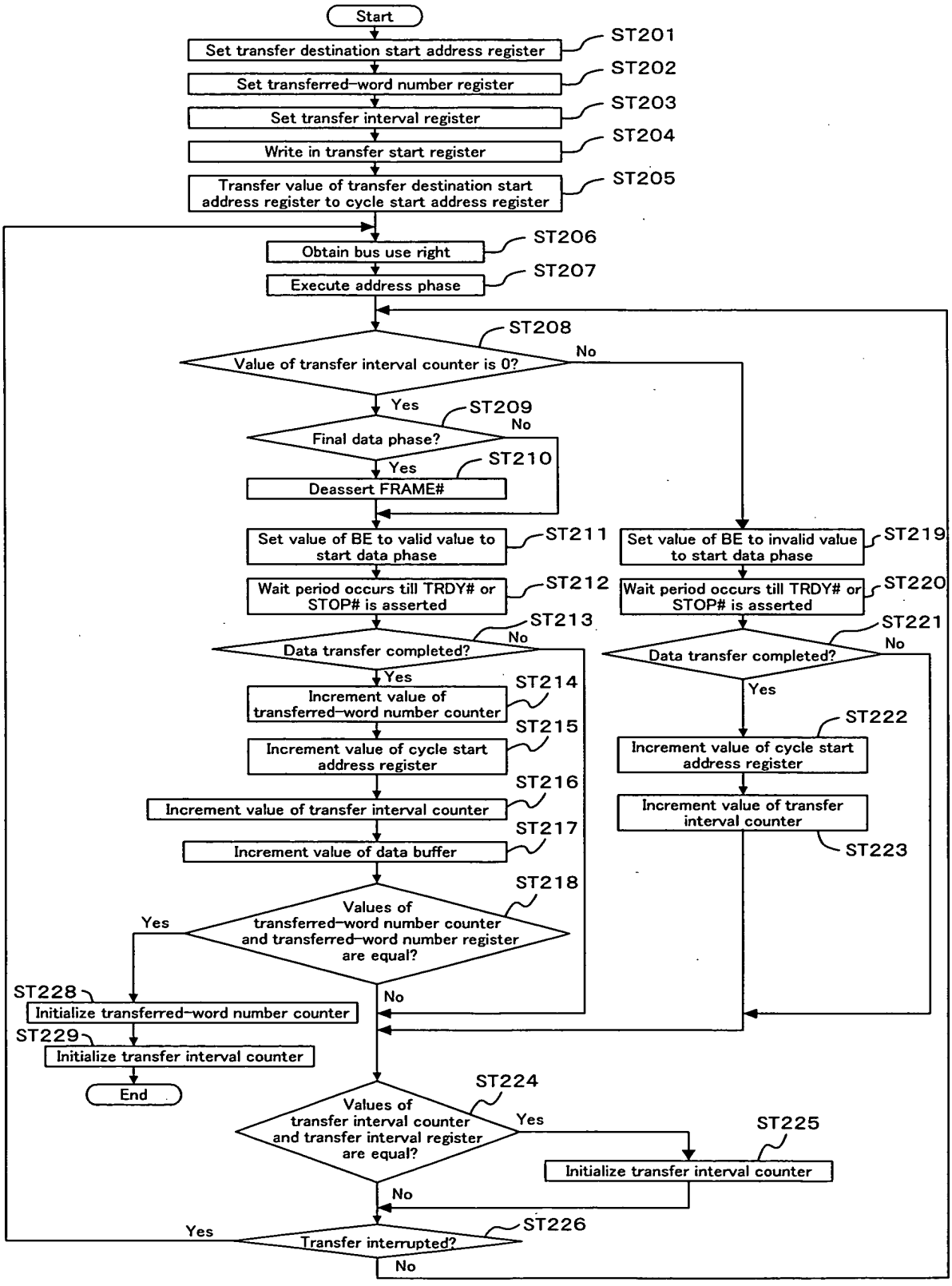

Start
Set transfer destination start address register
ST201
Set transferred-word number register
ST202
Set transfer interval register
ST203
Write in transfer start register
ST204
Transfer value of transfer destination start address register to cycle start address register
ST205
Obtain bus use right
ST206
Execute address phase
ST207
Value of transfer interval counter is 0?
ST208
No
Yes
Final data phase?
ST209
No
Yes
Deassert FRAME#
ST210
Set value of BE to valid value to start data phase
ST211
Wait period occurs till TRDY# or STOP# is asserted
ST212
Data transfer completed?
ST213
No
Yes
Increment value of transferred-word number counter
ST214
Increment value of cycle start address register
ST215
Increment value of transfer interval counter
ST216
Increment value of data buffer
ST217
Values of transferred-word number counter and transferred-word number register are equal?
ST218
Yes
No
Set value of BE to invalid value to start data phase
ST219
Wait period occurs till TRDY# or STOP# is asserted
ST220
Data transfer completed?
ST221
No
Yes
Increment value of cycle start address register
ST222
Increment value of transfer interval counter
ST223
Initialize transferred-word number counter
ST228
Initialize transfer interval counter
ST229
End
Values of transfer interval counter and transfer interval register are equal?
ST224
Yes
No
Initialize transfer interval counter
ST225
Transfer interrupted?
ST226
Yes
No

FIG. 3A

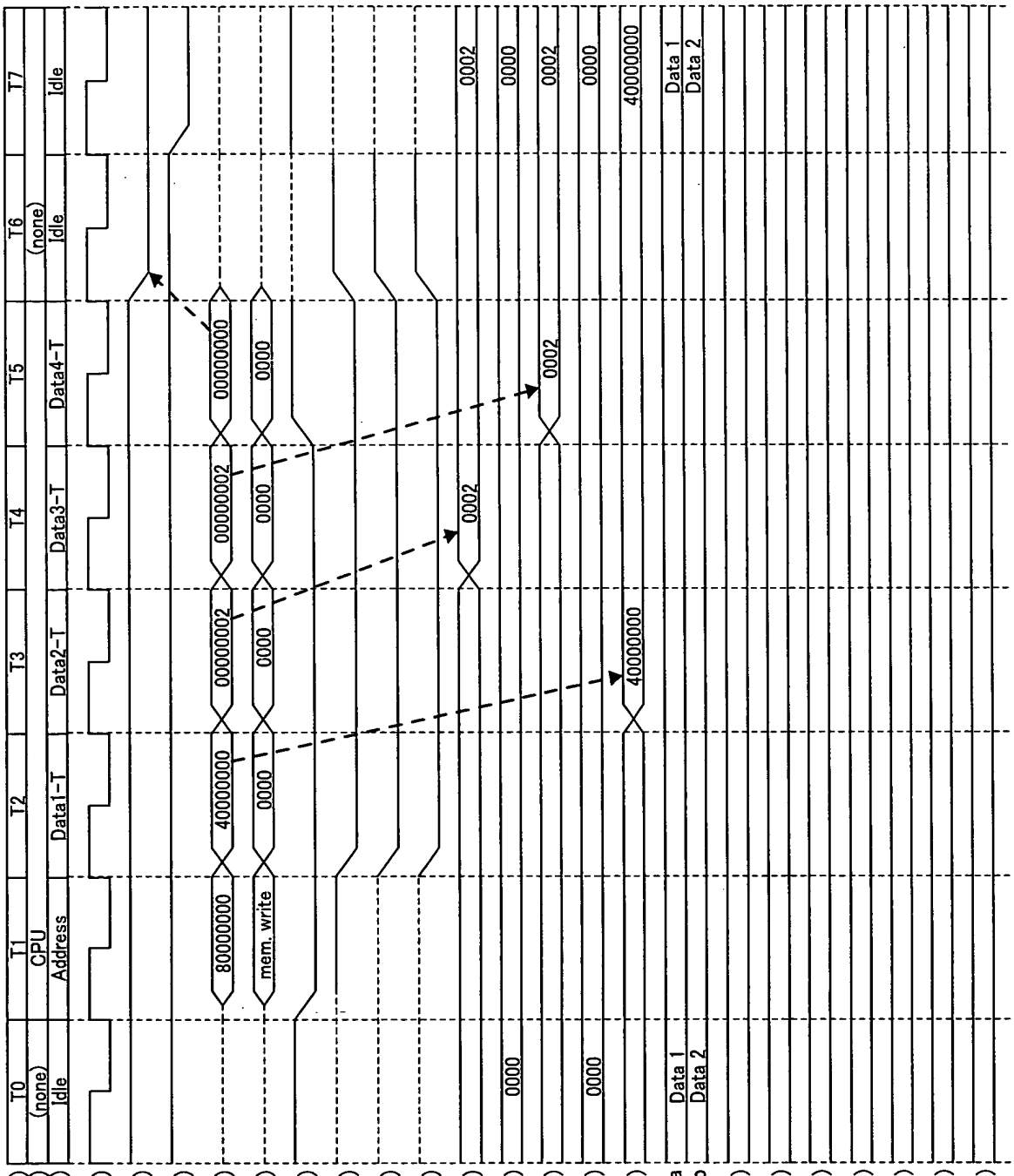

Time frame(300a)
Initiator(300b)
Bus status(300c)
Clock(clk)(301a)
REQ#(301b)
GNT#(301c)
ad[31:0](302)
c_be#(303)
frame#(304)
irdy#(305)
trdy#(306)
devsel#(307)
Transferred-word number register(308)
Transferred-word number counter(309)
Transfer interval register(310)
Transfer interval counter(311)
Transfer destination start address register(312)
Data buffer(313)
Address decoder(314)
Address register(315)
Data register(316)
Byte enable register(317)
40000000th address(318)
40000004th address(319)
40000008th address(320)
T0
T1
T2
T3
T4
T5
T6
T7
(none)
CPU
Idle
Address
Data1-T
Data2-T
Data3-T
Data4-T
Idle
(none)
Idle
80000000
40000000
00000002
00000002
00000000
mem. write
0000
0000
0000
0000
0000
0002
0002
0002
0000
0000
0000
40000000
40000000
a
b
Data 1
Data 2
Data 1
Data 2

FIG. 3B

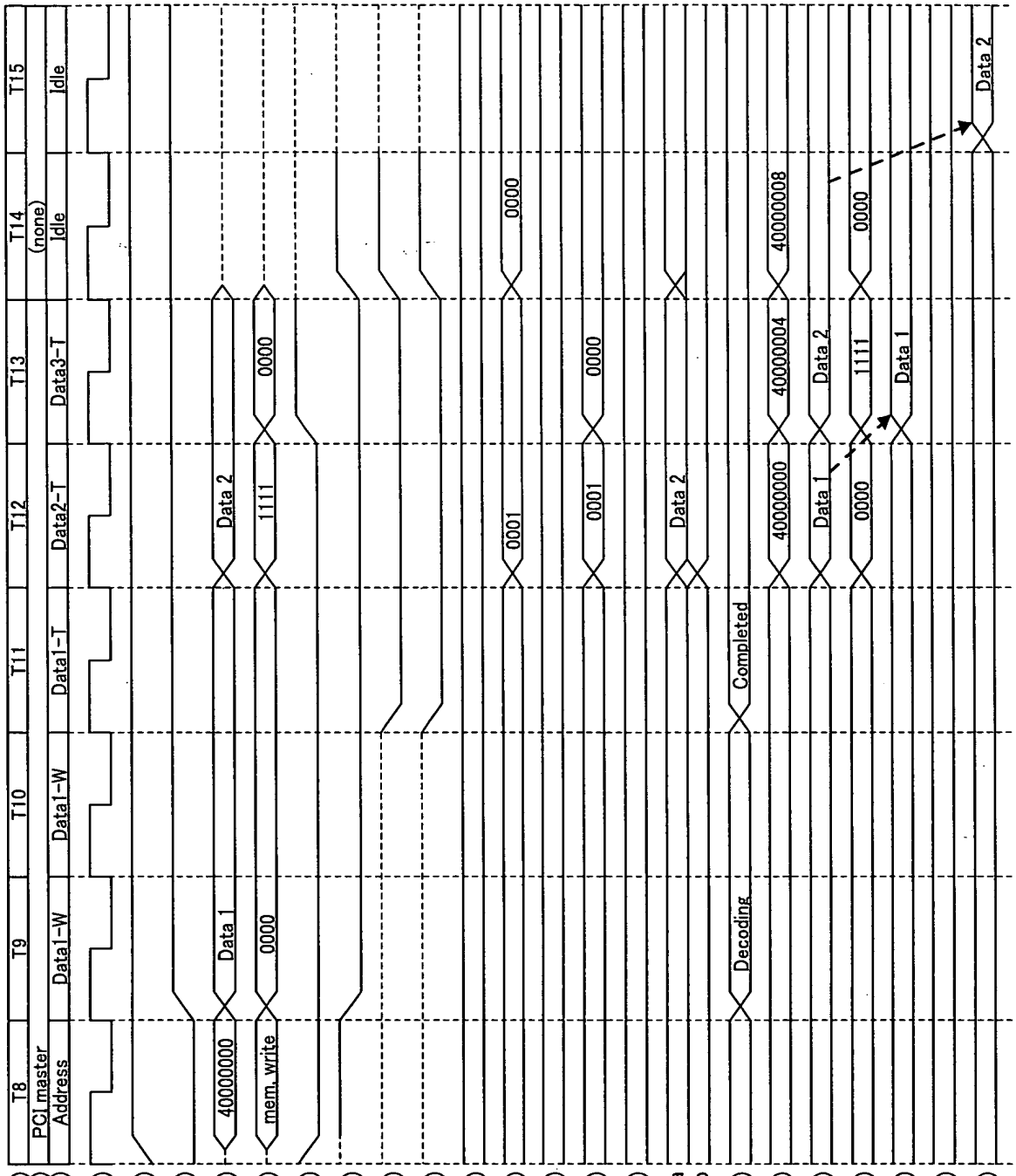

T8
T9
T10
T11
T12
T13
T14
T15
PCI master
Initiator
(none)
Address
Data1-W
Data1-W
Data1-T
Data2-T
Data3-T
Idle
Idle
Time frame(300a)
Initiator(300b)
Bus status(300c)
Clock(clk)(301a)
REQ#(301b)
GNT#(301c)
ad[31:0](302)
40000000
Data 1
Data 2
c_be#(303)
mem. write
0000
1111
0000
frame#(304)
irdy#(305)
trdy#(306)
devsel#(307)
Transferred-word number register(308)
Transferred-word number counter(309)
0001
0000
Transfer interval register(310)
Transfer interval counter(311)
0001
0000
Transfer destination start address register(312)
Data buffer(313)
a
b
Data 2
Address decoder(314)
Decoding
Completed
Address register(315)
40000000
40000004
40000008
Data register(316)
Data 1
Data 2
Byte enable register(317)
0000
1111
0000
40000000th address(318)
Data 1
40000004th address(319)
40000008th address(320)
Data 2

FIG. 4

Start address	End address	allocated to:
00000000	3fffffff	Memory 170
40000000	7fffffff	Memory 146
80000000	80000003	Transfer destination start address register 102
80000004	80000007	Transferred-word number register 103
80000008	8000000b	Transfer interval register 113
8000000c	8000000f	Transfer start register 106

FIG. 5

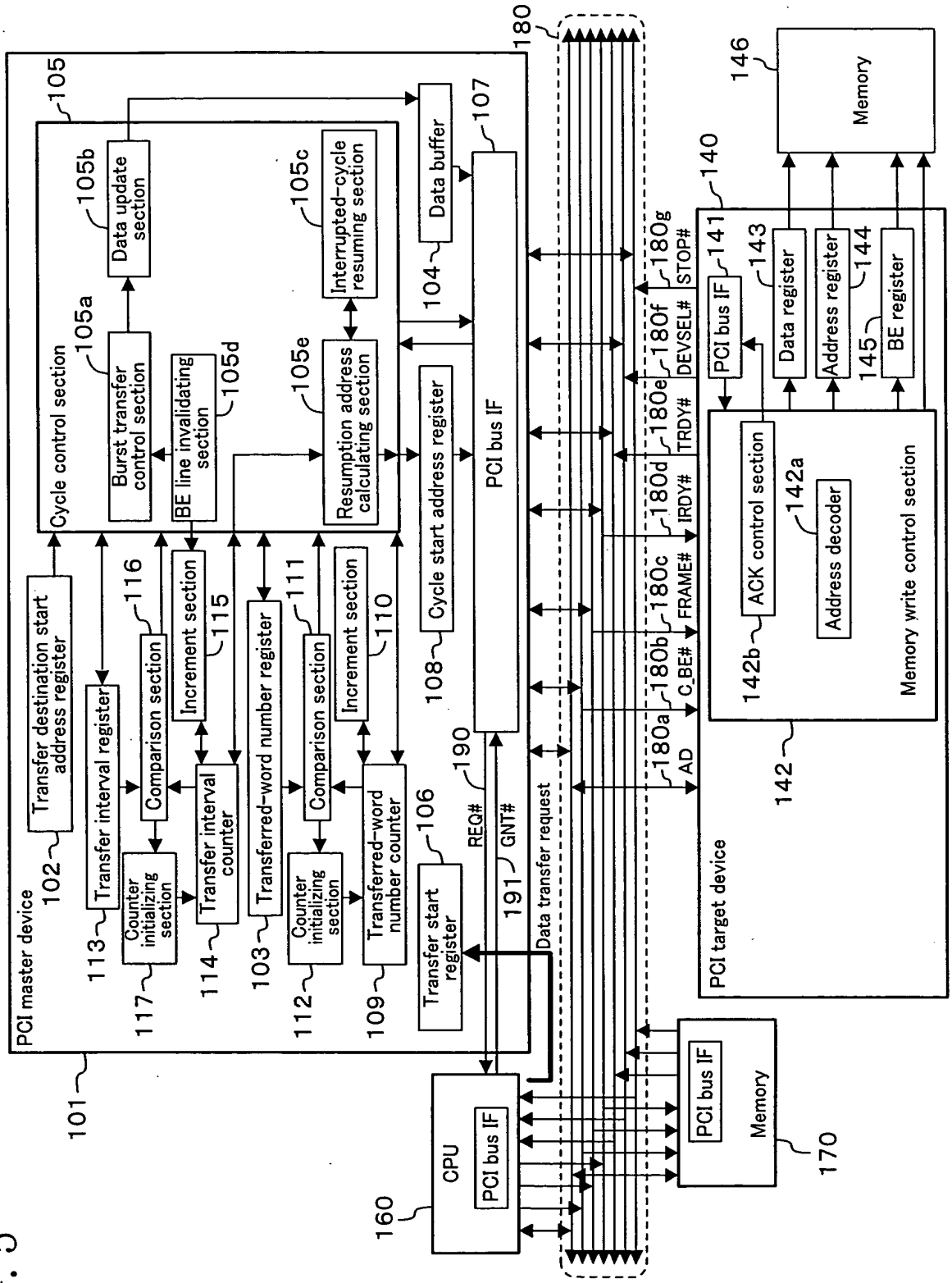

PCI master device
101
Cycle control section
105
Burst transfer control section
105a
Data update section
105b
Interrupted-cycle resuming section
105c
BE line invalidating section
105d
Resumption address calculating section
105e
Transfer destination start address register
102
Transfer interval register
113
Counter initializing section
117
Comparison section
116
Transfer interval counter
114
Increment section
115
Transferred-word number register
103
Counter initializing section
112
Comparison section
111
Transferred-word number counter
109
Increment section
110
Transfer start register
106
Cycle start address register
108
Data buffer
104
PCI bus IF
107
REQ#
190
GNT#
191
Data transfer request
180
180a AD
180b C_BE#
180c FRAME#
180d IRDY#
180e TRDY#
180f DEVSEL#
180g STOP#
CPU
160
PCI bus IF
Memory
170
PCI target device
142
PCI bus IF
141
Data register
143
Address register
144
BE register
145
ACK control section
142b
Address decoder
142a
Memory write control section
140
Memory
146

FIG. 6

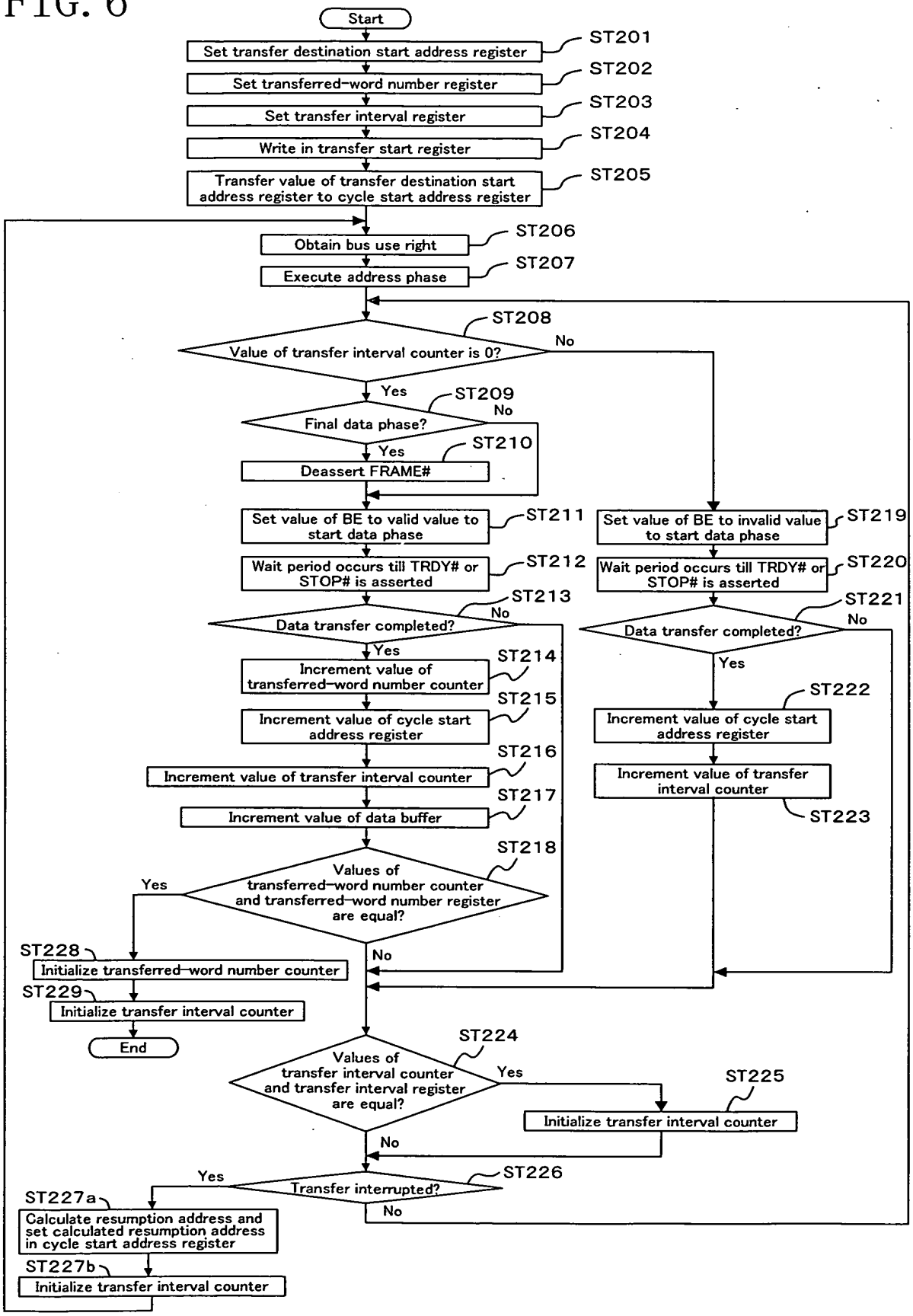

Start
Set transfer destination start address register
ST201
Set transferred-word number register
ST202
Set transfer interval register
ST203
Write in transfer start register
ST204
Transfer value of transfer destination start address register to cycle start address register
ST205
Obtain bus use right
ST206
Execute address phase
ST207
ST208
Value of transfer interval counter is 0?
No
Yes
ST209
Final data phase?
No
Yes
ST210
Deassert FRAME#
Set value of BE to valid value to start data phase
ST211
Wait period occurs till TRDY# or STOP# is asserted
ST212
ST213
Data transfer completed?
No
Yes
ST214
Increment value of transferred-word number counter
ST215
Increment value of cycle start address register
ST216
Increment value of transfer interval counter
ST217
Increment value of data buffer
ST218
Values of transferred-word number counter and transferred-word number register are equal?
Yes
No
Set value of BE to invalid value to start data phase
ST219
Wait period occurs till TRDY# or STOP# is asserted
ST220
ST221
Data transfer completed?
No
Yes
ST222
Increment value of cycle start address register
Increment value of transfer interval counter
ST223
ST228
Initialize transferred-word number counter
ST229
Initialize transfer interval counter
End
ST224
Values of transfer interval counter and transfer interval register are equal?
Yes
No
ST225
Initialize transfer interval counter
ST226
Transfer interrupted?
Yes
No
ST227a
Calculate resumption address and set calculated resumption address in cycle start address register
ST227b
Initialize transfer interval counter

FIG. 7

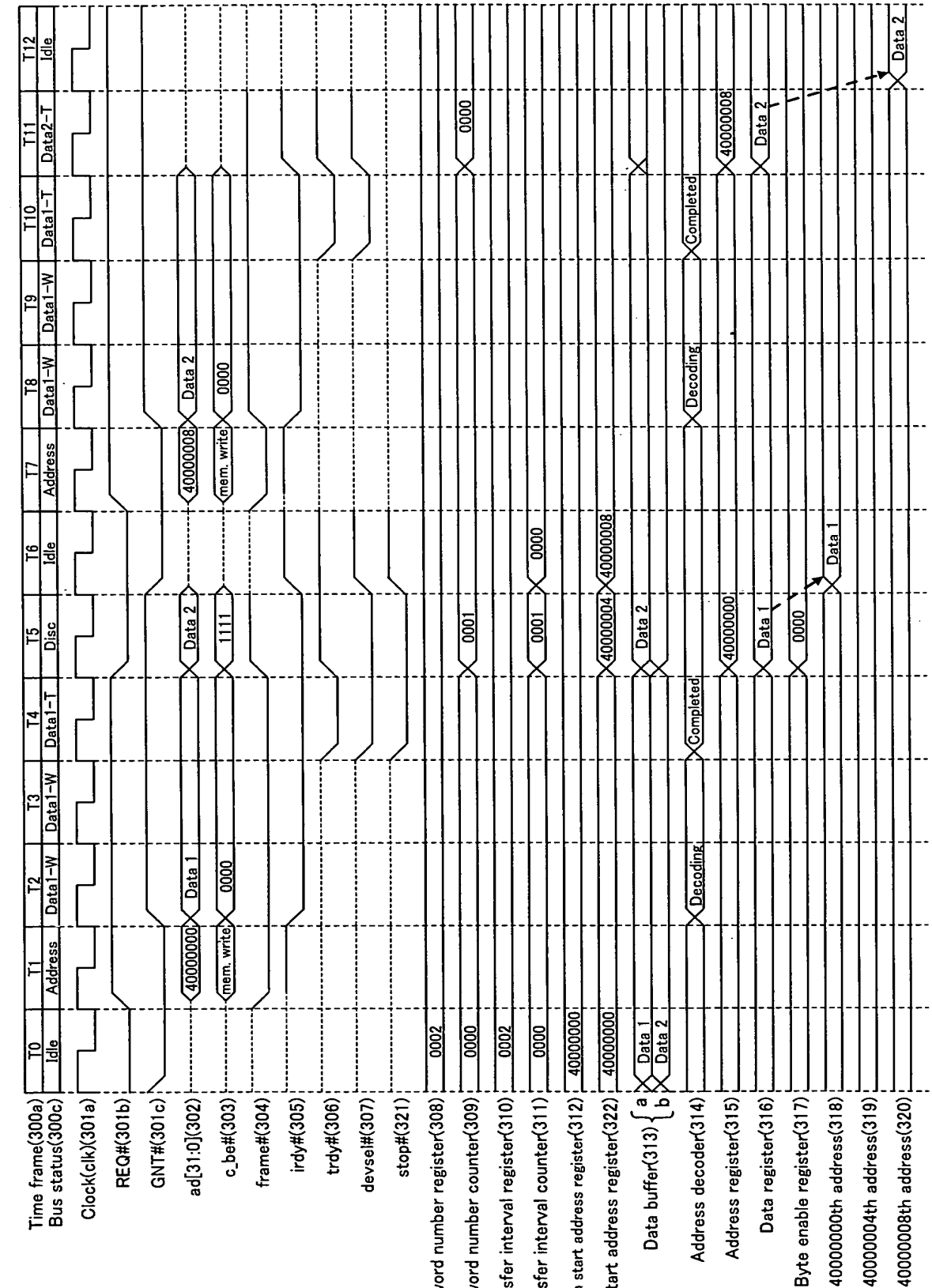

Time frame(300a)
Bus status(300c)
Clock(clk)(301a)
REQ#(301b)
GNT#(301c)
ad[31:0](302)
c_be#(303)
frame#(304)
irdy#(305)
trdy#(306)
devsel#(307)
stop#(321)
Transferred-word number register(308)
Transferred-word number counter(309)
Transfer interval register(310)
Transfer interval counter(311)
Transfer destination start address register(312)
Cycle start address register(322)
Data buffer(313)
a
b
Address decoder(314)
Address register(315)
Data register(316)
Byte enable register(317)
40000000h address(318)
40000004h address(319)
40000008h address(320)
T0
Idle
T1
Address
T2
Data1-W
T3
Data1-W
T4
Data1-T
T5
Disc
T6
Idle
T7
Address
T8
Data1-W
T9
Data1-W
T10
Data1-T
T11
Data2-T
T12
Idle
40000000
mem. write
0000
0002
0000
0001
0000
40000004
40000008
Data 1
Data 2
Decoding
Completed
40000000
40000008
0000
1111
Data 1
Data 2

FIG. 8A

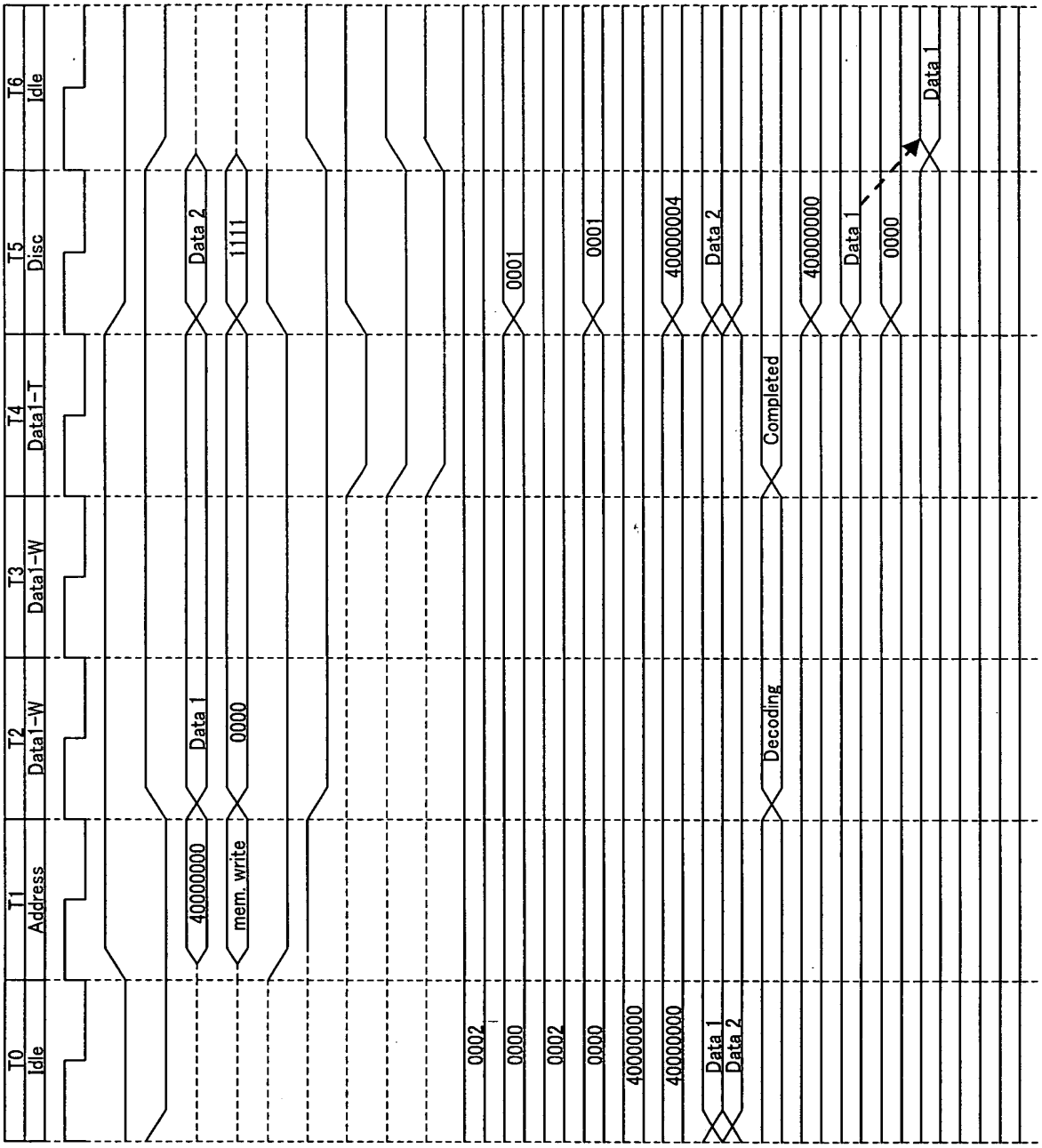

T0
T1
T2
T3
T4
T5
T6
Idle
Address
Data1-W
Data1-W
Data1-T
Disc
Idle
Time frame(300a)
Bus status(300c)
Clock(clk)(301a)
REQ#(301b)
GNT#(301c)
ad[31:0](302)
c_be#(303)
frame#(304)
irdy#(305)
trdy#(306)
devsel#(307)
stop#(321)
Transferred-word number register(308)
Transferred-word number counter(309)
Transfer interval register(310)
Transfer interval counter(311)
Transfer destination start address register(312)
Cycle start address register(322)
Data buffer(313)
a
b
Address decoder(314)
Address register(315)
Data register(316)
Byte enable register(317)
40000000th address(318)
40000004th address(319)
40000008th address(320)
40000000
mem. write
Data 1
Data 2
0000
1111
0002
0000
0001
0000
0002
0000
0001
40000000
40000000
40000004
Data 1
Data 2
Decoding
Completed
40000000
Data 1
0000
Data 1

FIG. 8B

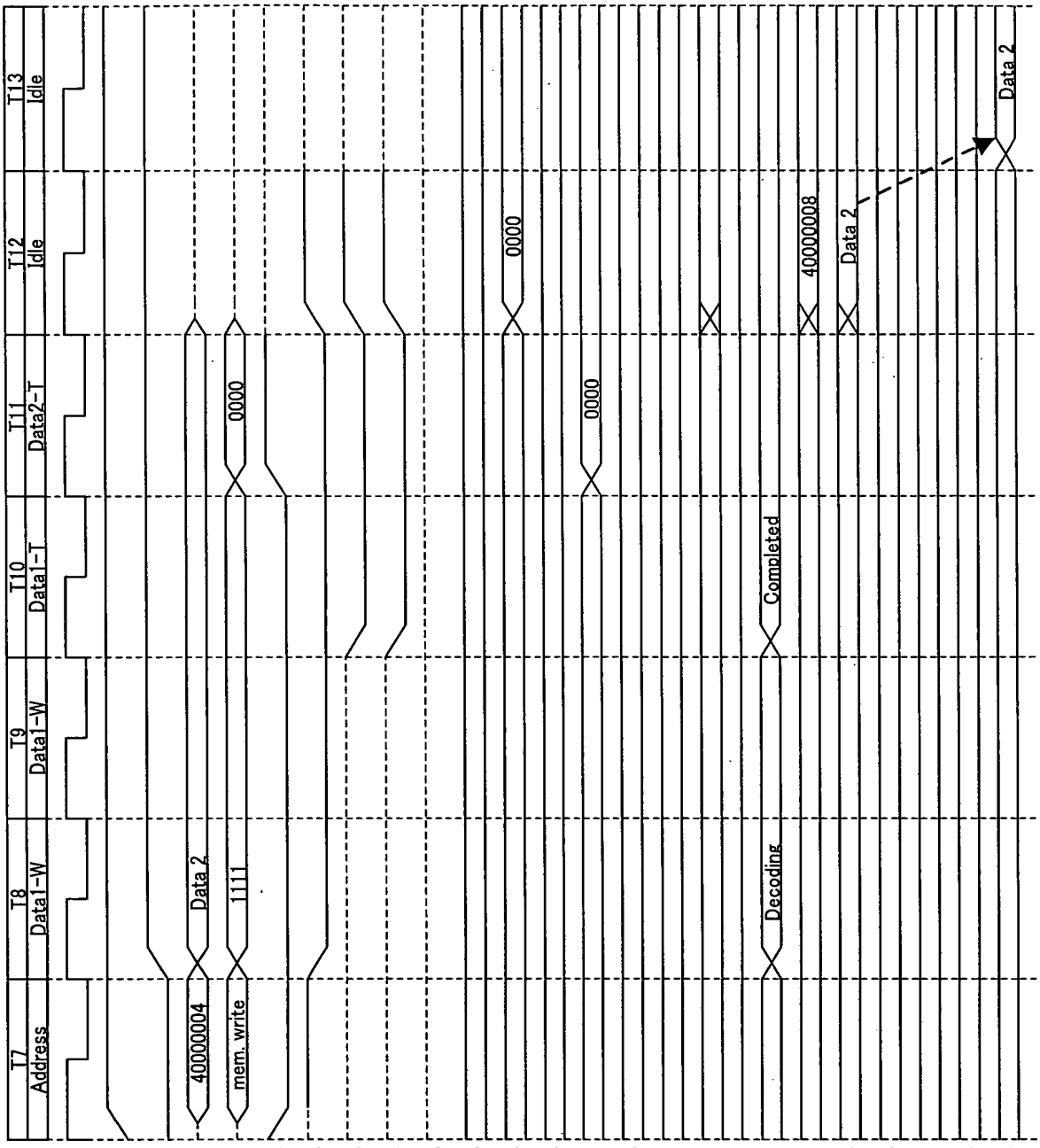

Time frame(300a)
Bus status(300c)
T7
Address
T8
Data1-W
T9
Data1-W
T10
Data1-T
T11
Data2-T
T12
Idle
T13
Idle
Clock(clk)(301a)
REQ#(301b)
GNT#(301c)
ad[31:0](302)
40000004
Data 2
c_be#(303)
mem. write
1111
0000
frame#(304)
irdy#(305)
trdy#(306)
devsel#(307)
stop#(321)
Transferred-word number register(308)
Transferred-word number counter(309)
0000
Transfer interval register(310)
Transfer interval counter(311)
0000
Transfer destination start address register(312)
Cycle start address register(322)
Data buffer(313)
a
b
Address decoder(314)
Decoding
Completed
Address register(315)
40000008
Data register(316)
Data 2
Byte enable register(317)
40000000th address(318)
40000004th address(319)
40000008th address(320)
Data 2

FIG. 9

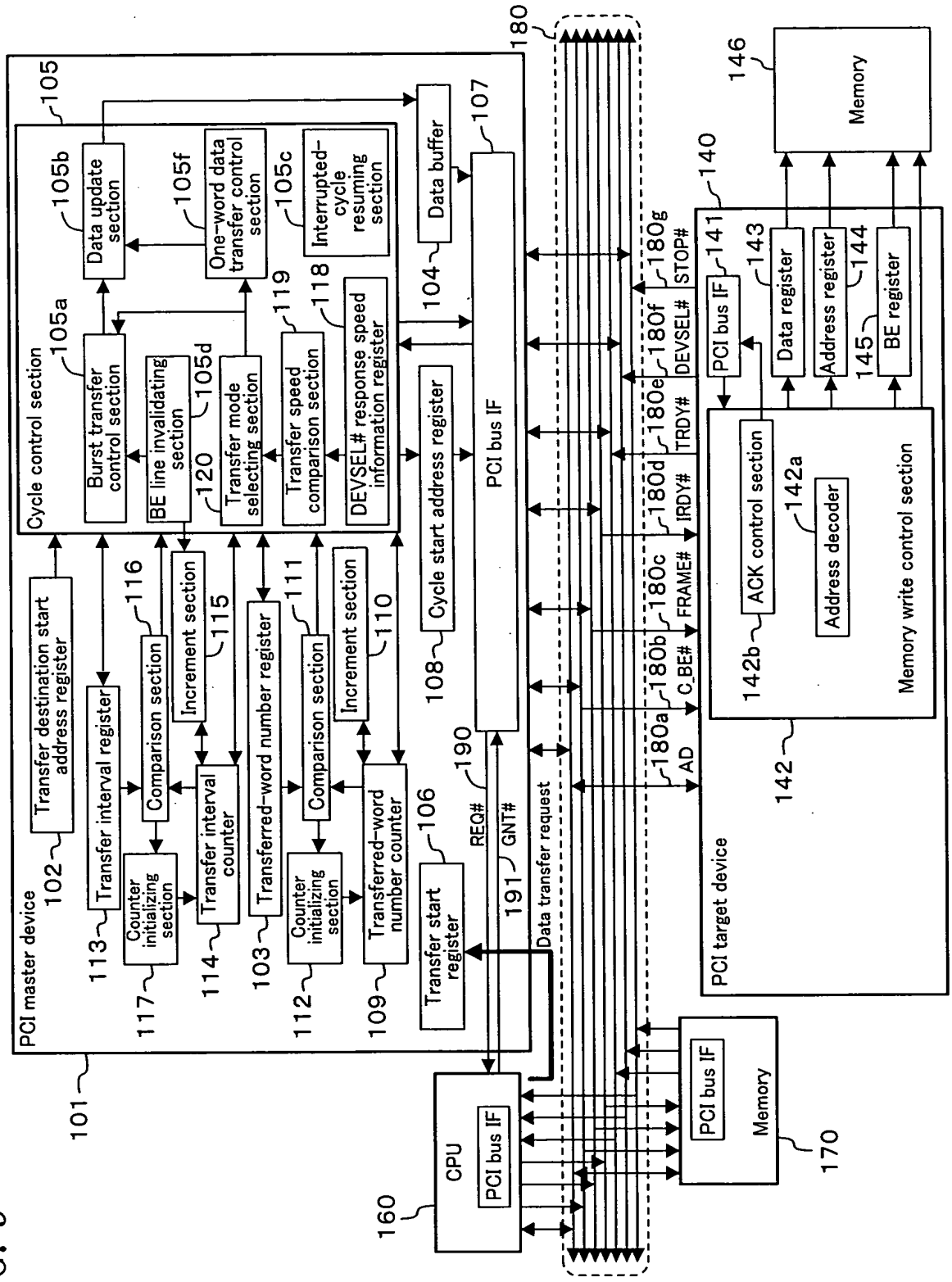

PCI master device
101
Cycle control section
105
Burst transfer control section
105a
Data update section
105b
Interrupted-cycle resuming section
105c
One-word data transfer control section
105f
BE line invalidating section
105d
Transfer mode selecting section
120
Transfer speed comparison section
119
DEVSEL# response speed information register
118
Data buffer
104
Transfer destination start address register
102
Transfer interval register
113
Counter initializing section
117
Comparison section
116
Increment section
115
Transfer interval counter
114
Transferred-word number register
103
Counter initializing section
112
Comparison section
111
Increment section
110
Transferred-word number counter
109
Transfer start register
106
Cycle start address register
108
PCI bus IF
107
REQ#
190
GNT#
191
Data transfer request
180
AD
180a
C_BE#
180b
FRAME#
180c
IRDY#
180d
TRDY#
180e
DEVSEL#
180f
STOP#
180g
CPU
160
PCI bus IF
Memory
170
PCI target device
142
PCI bus IF
141
ACK control section
142b
Address decoder
142a
Memory write control section
140
Data register
143
Address register
144
BE register
145
Memory
146

FIG. 10

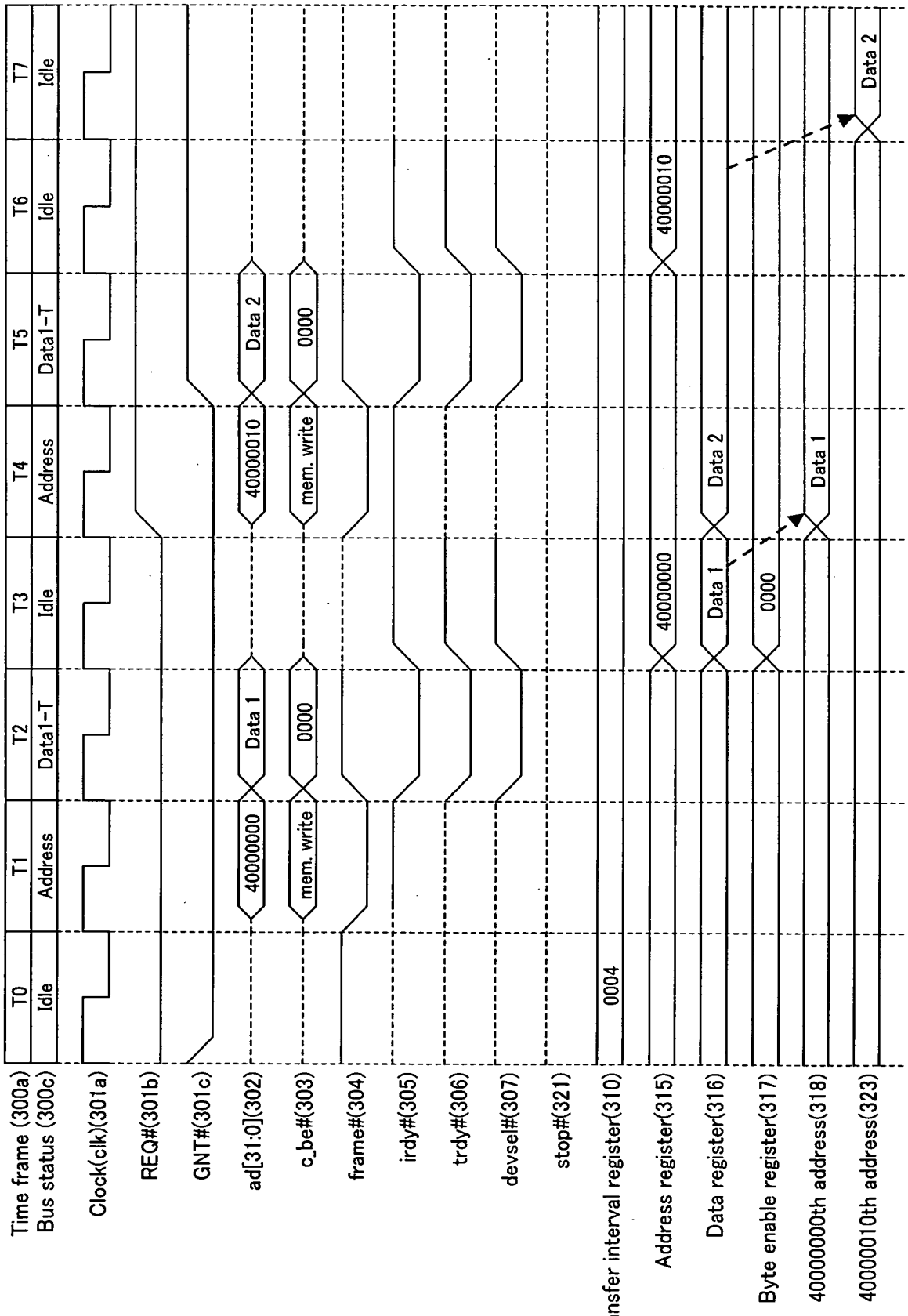

Time frame (300a)
Bus status (300c)
T0
Idle
T1
Address
T2
Data1-T
T3
Idle
T4
Address
T5
Data1-T
T6
Idle
T7
Idle
Clock(clk)(301a)
REQ#(301b)
GNT#(301c)
ad[31:0](302)
40000000
Data 1
40000010
Data 2
c_be#(303)
mem. write
0000
mem. write
0000
frame#(304)
irdy#(305)
trdy#(306)
devsel#(307)
stop#(321)
Transfer interval register(310)
0004
Address register(315)
40000000
40000010
Data register(316)
Data 1
Data 2
Byte enable register(317)
0000
Data 1
40000000th address(318)
40000010th address(323)
Data 2

FIG. 11

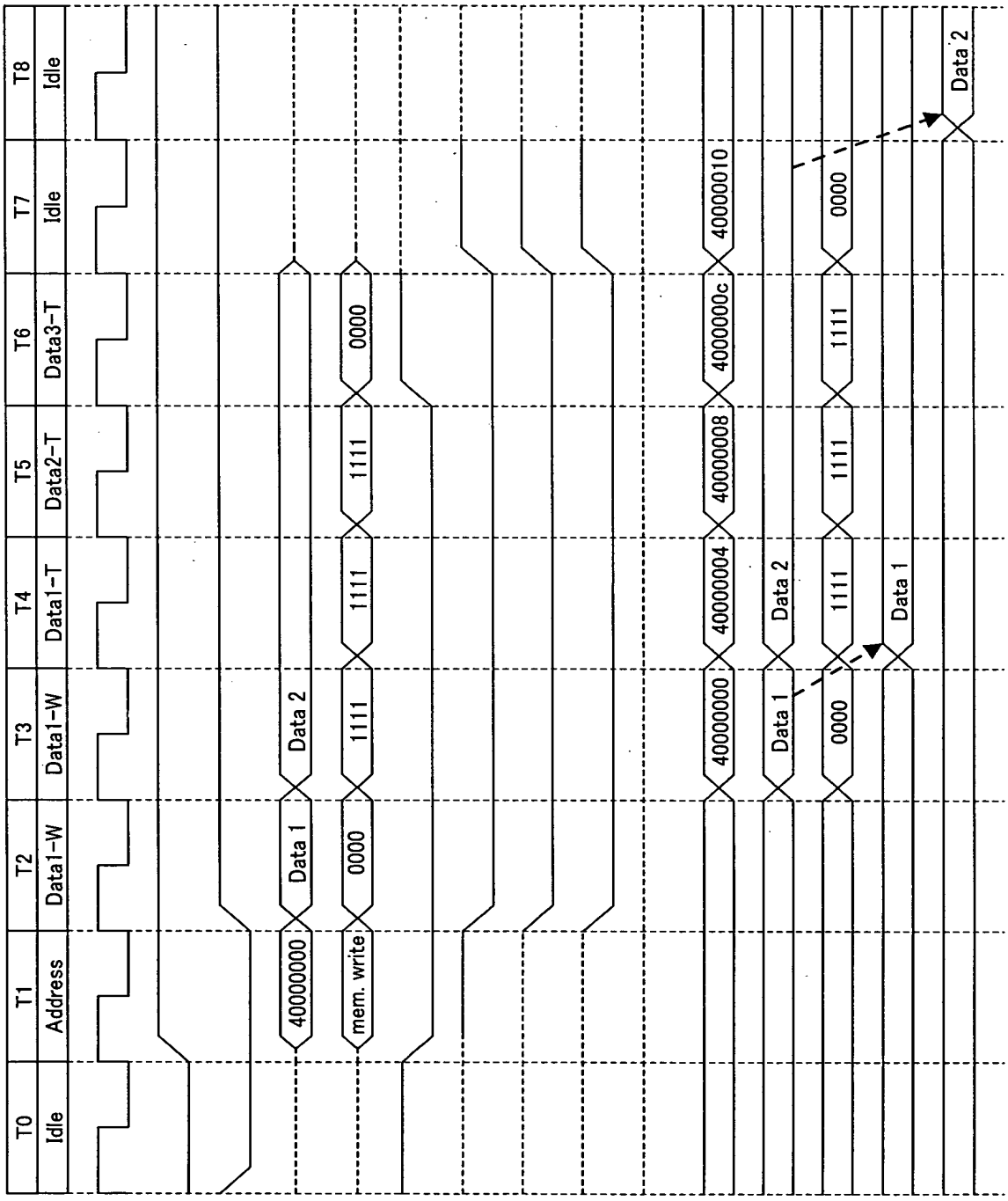

Time frame(300a)
Bus status(300c)
Clock(clk)(301a)
REQ#(301b)
GNT#(301c)
ad[31:0](302)
c_be#(303)
frame#(304)
irdy#(305)
trdy#(306)
devsel#(307)
stop#(321)
Address register(315)
Data register(316)
Byte enable register(317)
40000000th address(318)
40000010th address(323)
T0
Idle
T1
Address
T2
Data1-W
T3
Data1-W
T4
Data1-T
T5
Data2-T
T6
Data3-T
T7
Idle
T8
Idle
40000000
Data 1
Data 2
mem. write
0000
1111
1111
0000
1111
40000000
40000004
40000008
4000000c
40000010
Data 1
Data 2
0000
1111
1111
1111
0000
Data 1
Data 2

FIG. 12

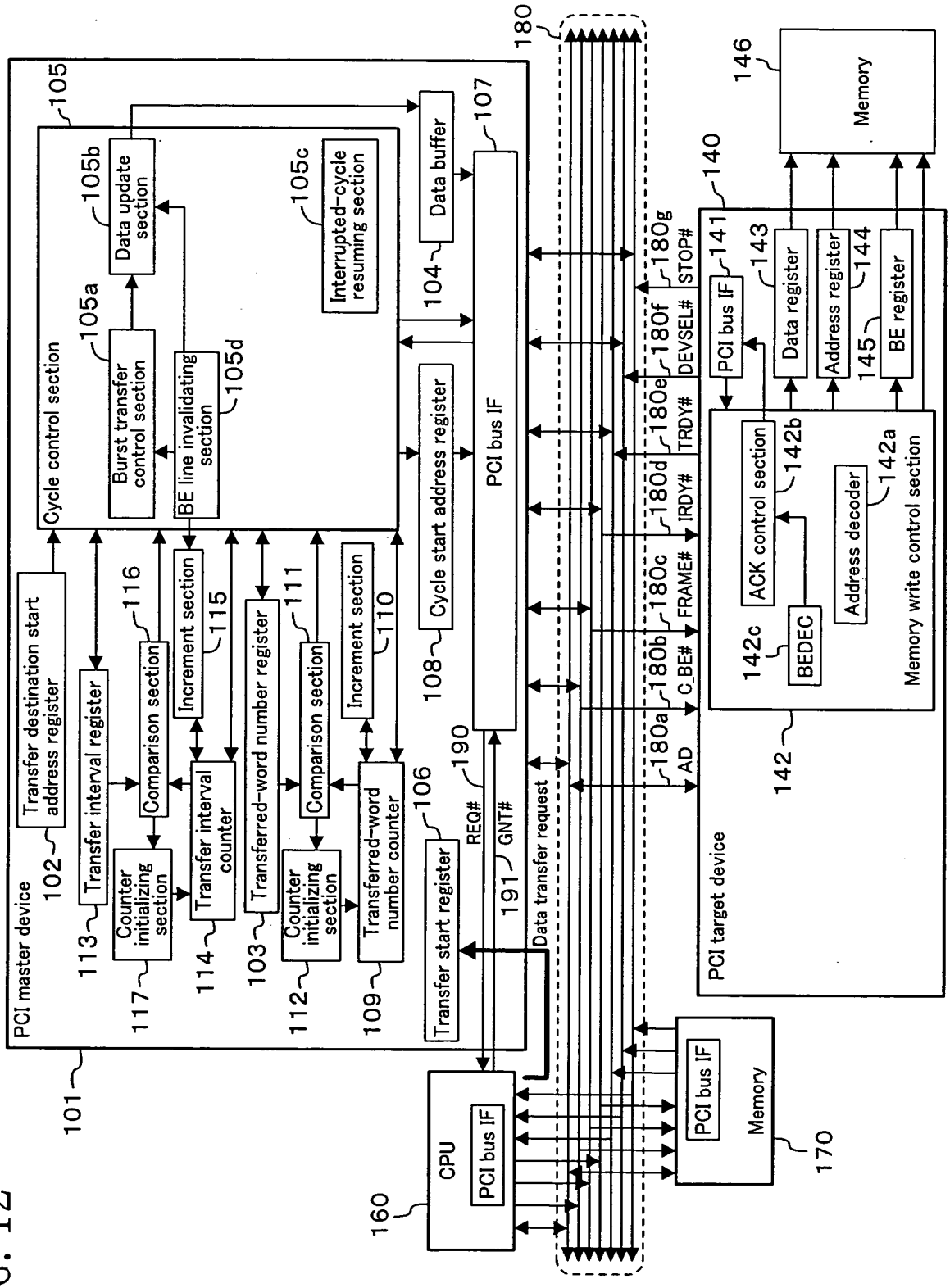

PCI master device
101
Cycle control section
105
Transfer destination start address register
102
Transfer interval register
113
Counter initializing section
117
Comparison section
116
Transfer interval counter
114
Increment section
115
Transferred-word number register
103
Counter initializing section
112
Comparison section
111
Transferred-word number counter
109
Increment section
110
Transfer start register
106
Burst transfer control section
105a
Data update section
105b
BE line invalidating section
105d
Interrupted-cycle resuming section
105c
Cycle start address register
108
Data buffer
104
PCI bus IF
107
180
REQ#
190
GNT#
191
Data transfer request
CPU
160
PCI bus IF
Memory
170
PCI bus IF
180a
AD
180b
C_BE#
180c
FRAME#
180d
IRDY#
180e
TRDY#
180f
DEVSEL#
180g
STOP#
PCI target device
142
PCI bus IF
141
ACK control section
142b
BEDEC
142c
Address decoder
142a
Memory write control section
140
Data register
143
Address register
144
BE register
145
Memory
146

FIG. 13

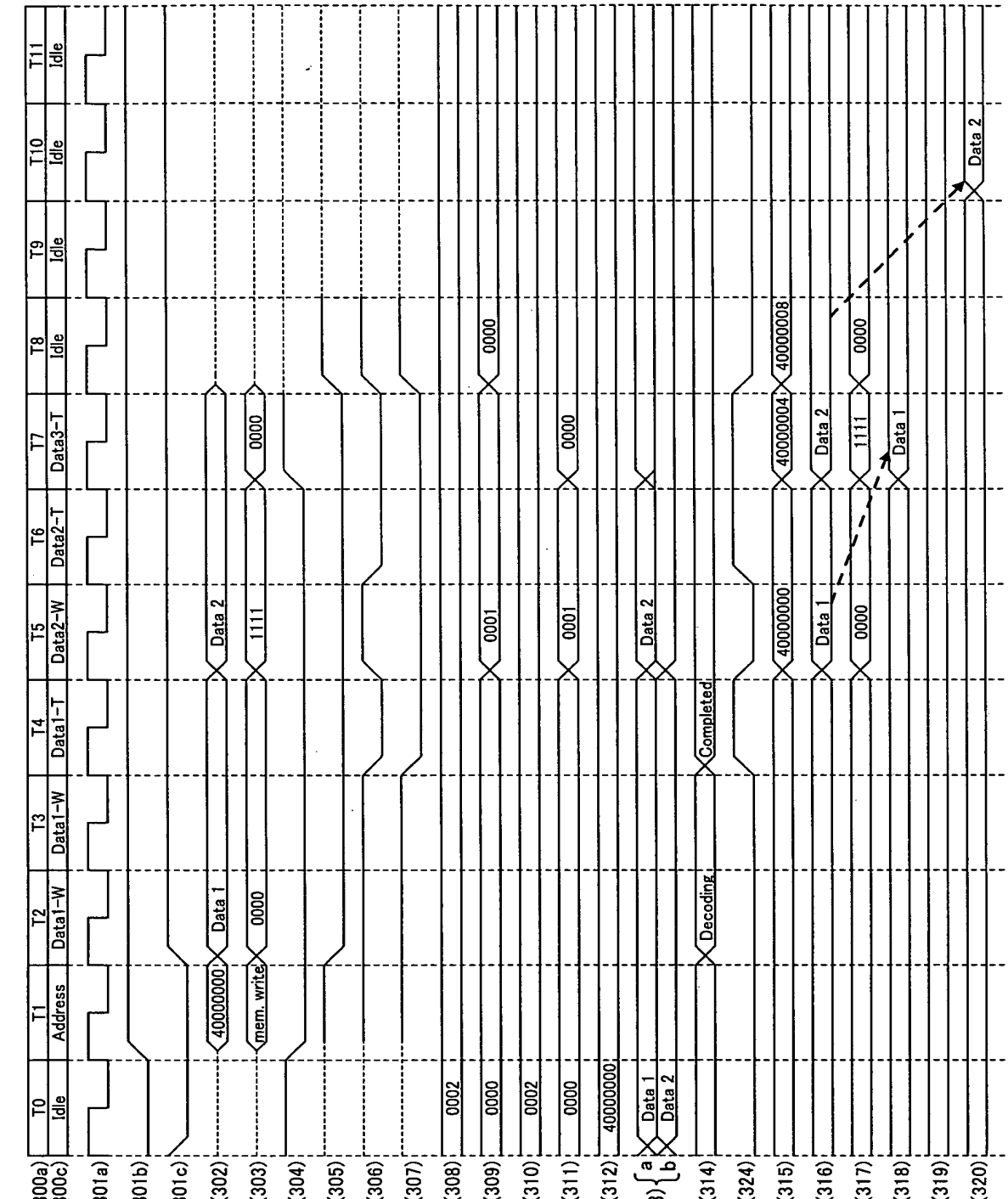

Time frame(300a)
Bus status(300c)
T0
Idle
T1
Address
T2
Data1-W
T3
Data1-W
T4
Data1-T
T5
Data2-W
T6
Data2-T
T7
Data3-T
T8
Idle
T9
Idle
T10
Idle
T11
Idle
Clock(clk)(301a)
REQ#(301b)
GNT#(301c)
ad[31:0](302)
40000000
Data 1
Data 2
c_be#(303)
mem. write
0000
1111
0000
frame#(304)
irdy#(305)
trdy#(306)
devsel#(307)
Transferred-word number register(308)
0002
Transferred-word number counter(309)
0000
0001
0000
Transfer interval register(310)
0002
Transfer interval counter(311)
0000
0001
0000
Transfer destination start address register(312)
40000000
Data buffer(313)
a
b
Data 1
Data 2
Data 2
Address decoder(314)
Decoding
Completed
Acknowledgement signal(324)
Address register(315)
40000000
40000004
40000008
Data register(316)
Data 1
Data 2
Byte enable register(317)
0000
1111
0000
40000000th address(318)
Data 1
40000004th address(319)
40000008th address(320)
Data 2

FIG. 14

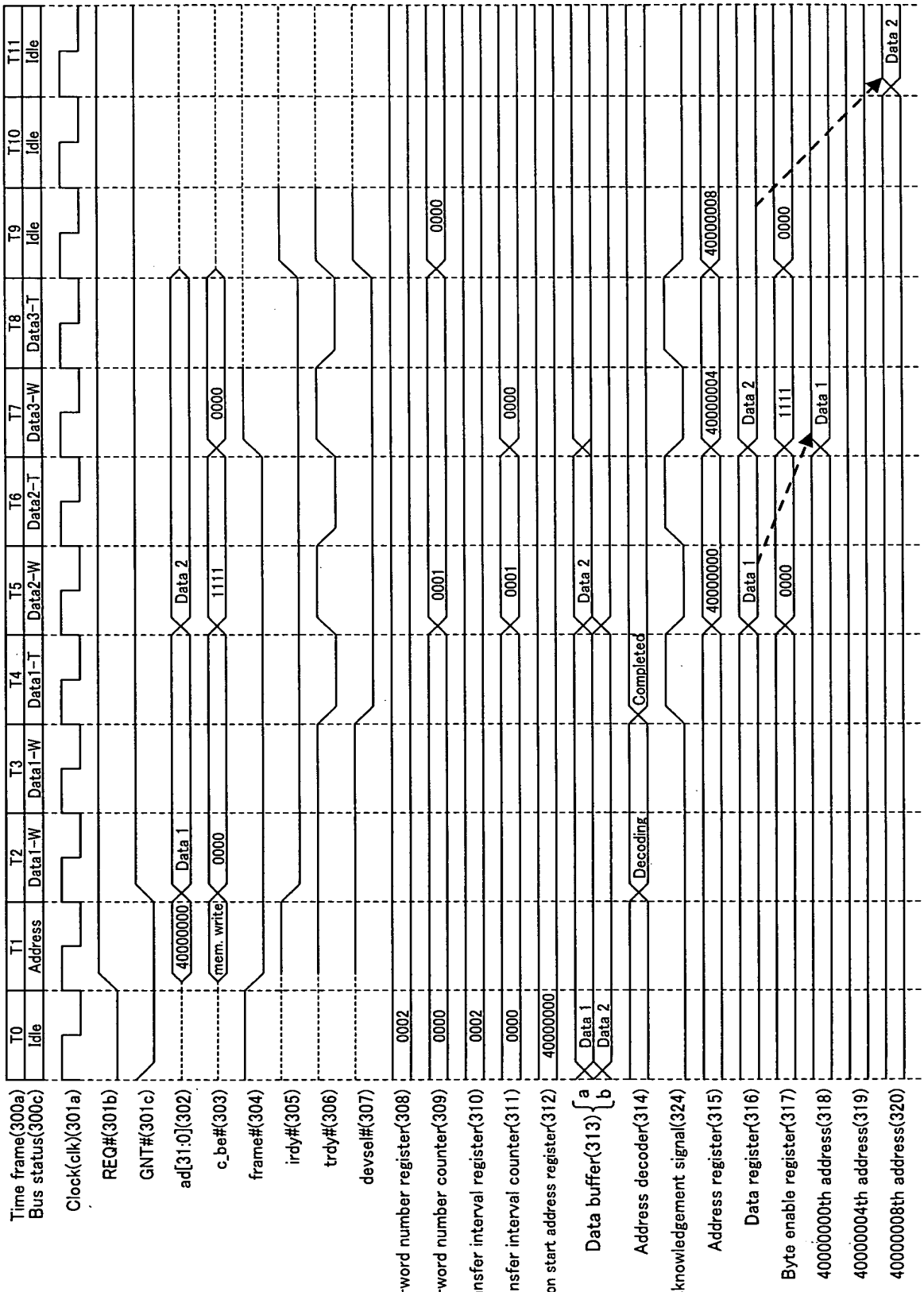

Time frame(300a)
Bus status(300c)
T0
Idle
T1
Address
T2
Data1-W
T3
Data1-W
T4
Data1-T
T5
Data2-W
T6
Data2-T
T7
Data3-W
T8
Data3-T
T9
Idle
T10
Idle
T11
Idle
Clock(clk)(301a)
REQ#(301b)
GNT#(301c)
ad[31:0](302)
40000000
Data 1
Data 2
c_be#(303)
mem. write
0000
1111
0000
frame#(304)
irdy#(305)
trdy#(306)
devsel#(307)
Transferred-word number register(308)
0002
Transferred-word number counter(309)
0000
0001
0000
Transfer interval register(310)
0002
Transfer interval counter(311)
0000
0001
0000
Transfer destination start address register(312)
40000000
Data buffer(313)
a
b
Data 1
Data 2
Data 2
Address decoder(314)
Decoding
Completed
Acknowledgement signal(324)
Address register(315)
40000000
40000004
40000008
Data register(316)
Data 1
Data 2
Byte enable register(317)
0000
1111
0000
40000000th address(318)
Data 1
40000004th address(319)
40000008th address(320)
Data 2

FIG. 15

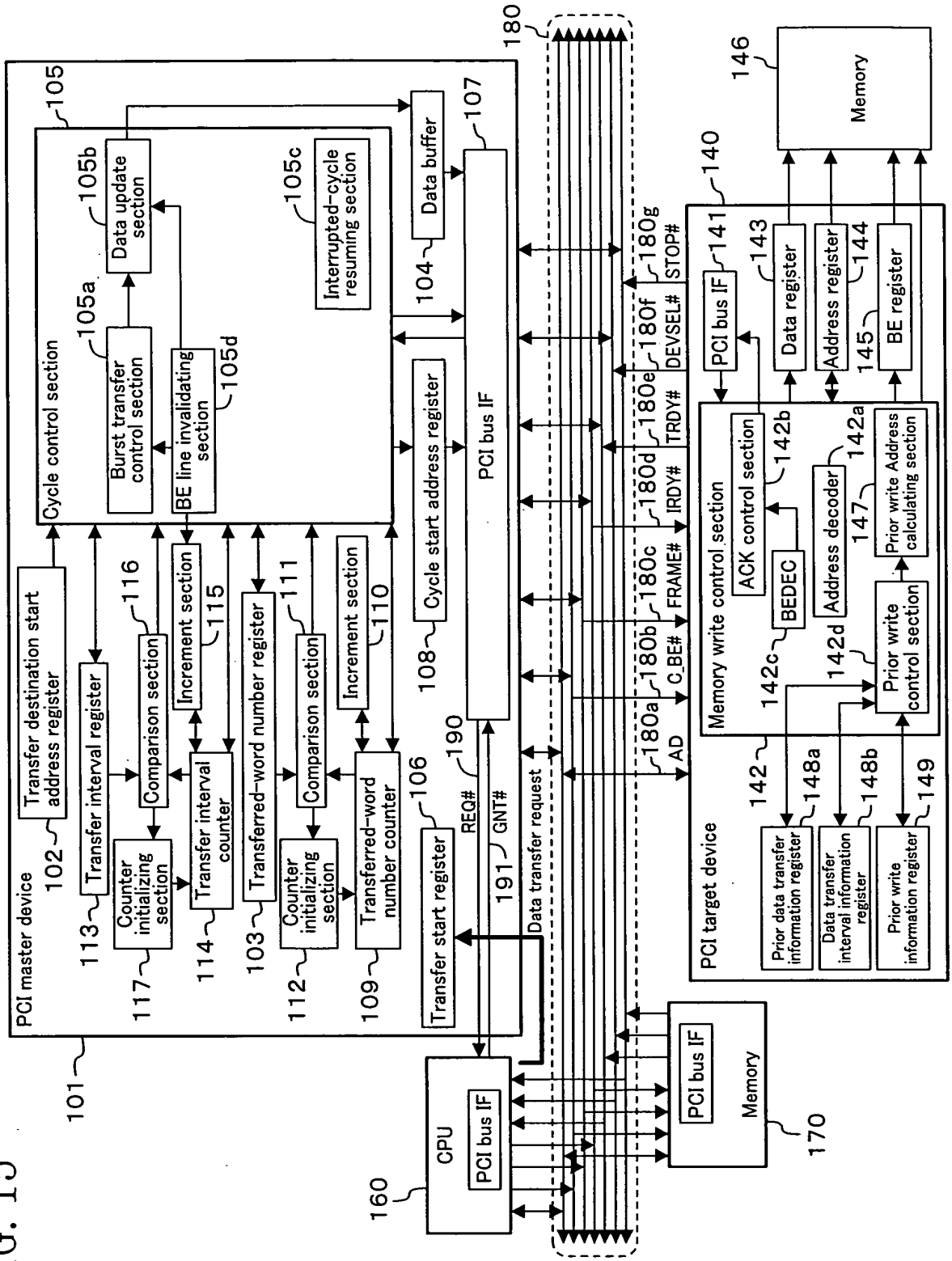

PCI master device
101
Cycle control section
105
Burst transfer control section
105a
Data update section
105b
Interrupted-cycle resuming section
105c
BE line invalidating section
105d
Transfer destination start address register
102
Transfer interval register
113
Counter initializing section
117
Comparison section
116
Transfer interval counter
114
Increment section
115
Transferred-word number register
103
Counter initializing section
112
Comparison section
111
Transferred-word number counter
109
Increment section
110
Transfer start register
106
Cycle start address register
108
Data buffer
107
PCI bus IF
104
180
REQ#
190
GNT#
191
Data transfer request
CPU
160
PCI bus IF
Memory
170
180a AD
180b C_BE#
180c FRAME#
180d IRDY#
180e TRDY#
180f DEVSEL#
180g STOP#
PCI target device
142
Memory write control section
142c
ACK control section
142b
BEDEC
Address decoder
142d
Prior write control section
147
Prior write Address calculating section
142a
Prior data transfer information register
148a
Data transfer interval information register
148b
Prior write information register
149
PCI bus IF
141
Data register
143
Address register
144
BE register
145
140
Memory
146

FIG. 16

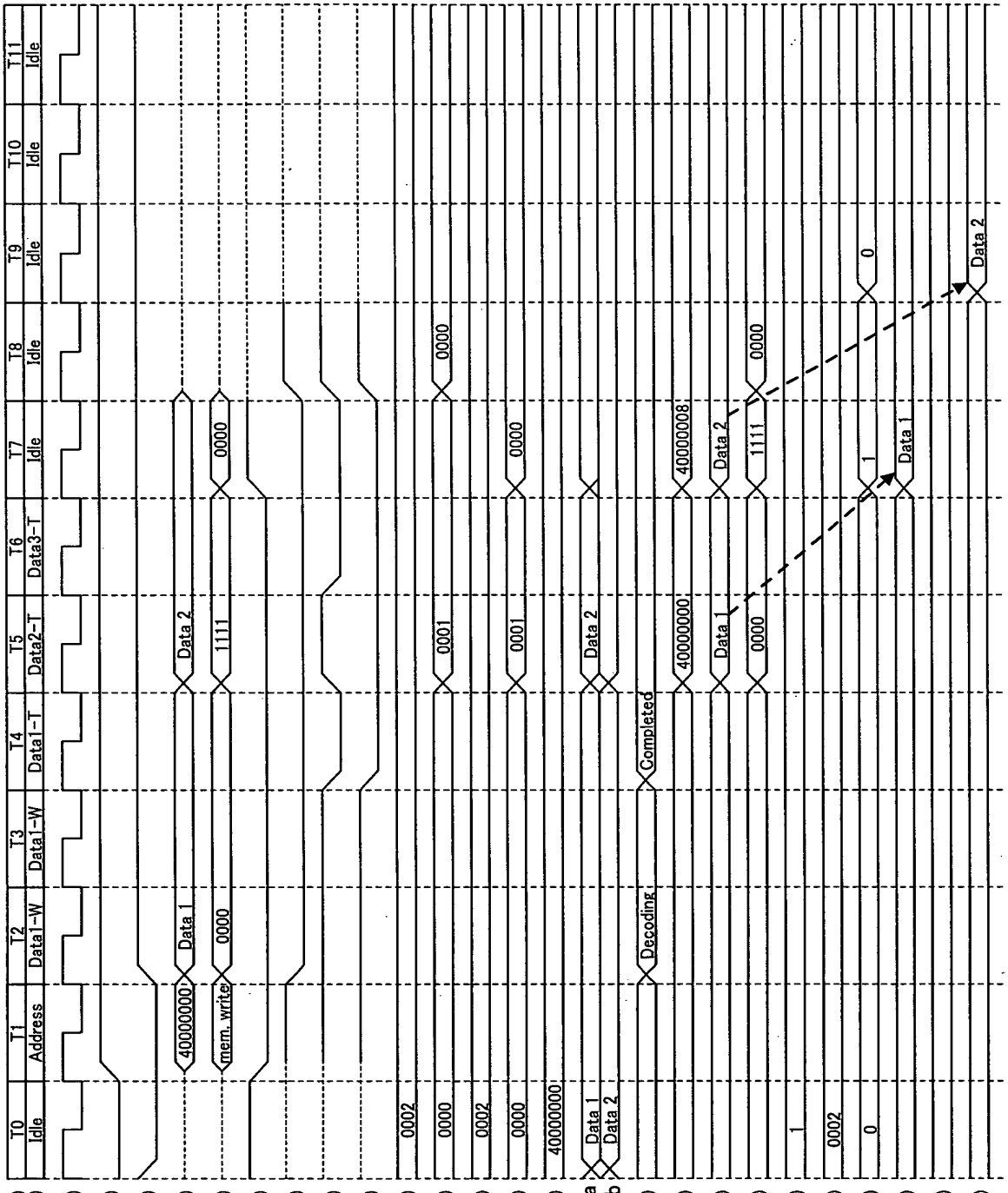

Time frame(300a)
Bus status(300c)
Clock(clk)(301a)
REQ#(301b)
GNT#(301c)
ad[31:0](302)
c_be#(303)
frame#(304)
irdy#(305)
trdy#(306)
devsel#(307)
Transferred-word number register(308)
Transferred-word number counter(309)
Transfer interval register(310)
Transfer interval counter(311)
Transfer destination start address register(312)
Data buffer(313)
Address decoder(314)
Address register(315)
Data register(316)
Byte enable register(317)
Prior data transfer information register(325)
Data transfer interval information register(326)
Prior write information register(327)
40000000th address(318)
40000004th address(319)
40000008th address(320)
T0
Idle
T1
Address
T2
Data1-W
T3
Data1-W
T4
Data1-T
T5
Data2-T
T6
Data3-T
T7
Idle
T8
Idle
T9
Idle
T10
Idle
T11
Idle
40000000
Data 1
0000
mem. write
Data 2
1111
0000
0002
0000
0002
0000
40000000
Data 1
Data 2
a
b
Decoding
Completed
Data 2
0001
0001
40000000
Data 1
0000
40000008
Data 2
1111
0000
1
1
Data 1
0
0
Data 2

FIG. 17

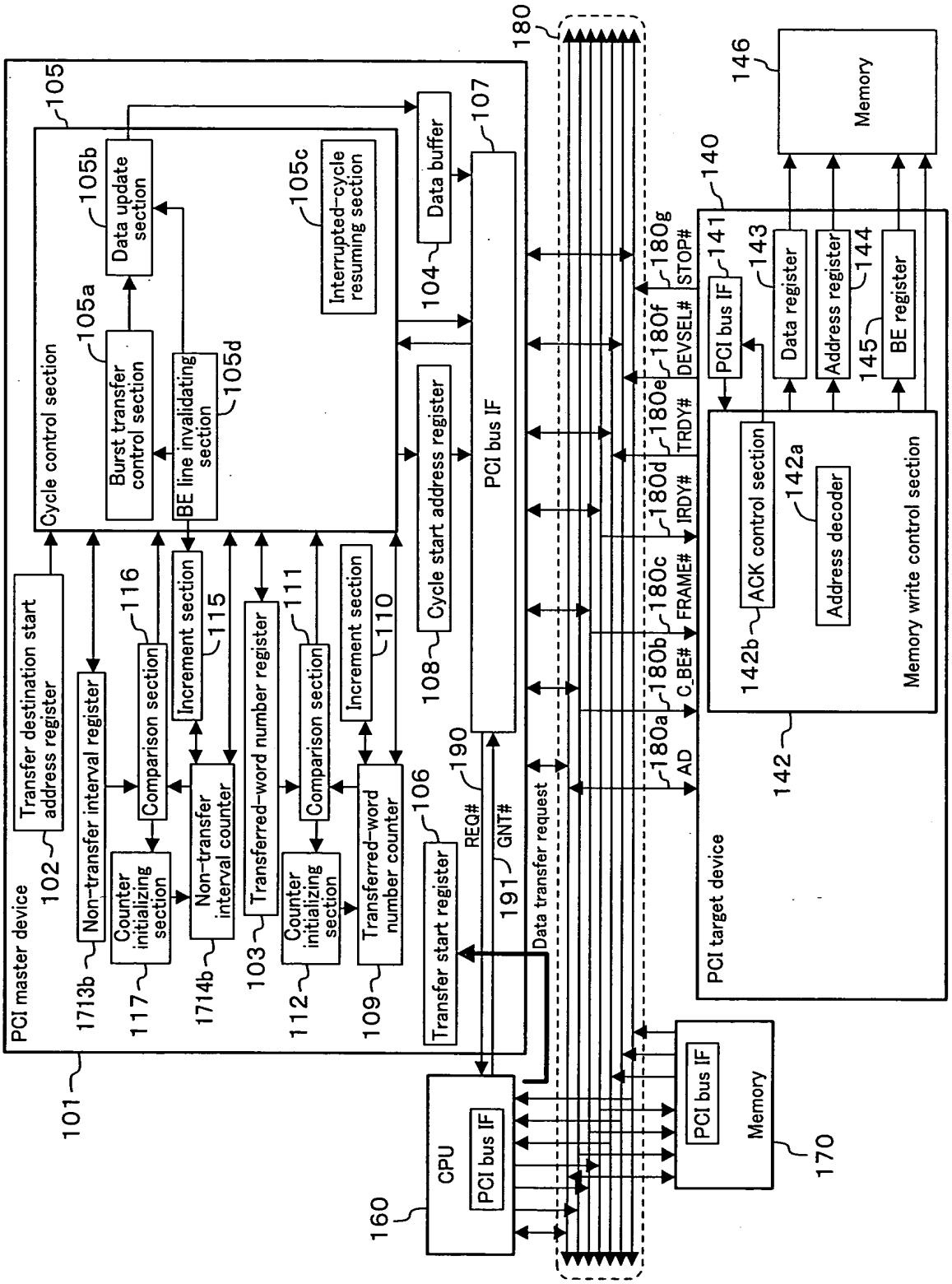

PCI master device
101
Cycle control section
105
Burst transfer control section
105a
Data update section
105b
Interrupted-cycle resuming section
105c
BE line invalidating section
105d
Transfer destination start address register
102
Non-transfer interval register
1713b
Counter initializing section
117
Comparison section
116
Increment section
115
Non-transfer interval counter
1714b
Transferred-word number register
103
Counter initializing section
112
Comparison section
111
Increment section
110
Transferred-word number counter
109
Transfer start register
106
Cycle start address register
108
Data buffer
107
PCI bus IF
104
180
REQ#
190
GNT#
191
Data transfer request
180a
AD
180b
C_BE#
180c
FRAME#
180d
IRDY#
180e
TRDY#
180f
DEVSEL#
180g
STOP#
CPU
160
PCI bus IF
Memory
170
PCI target device
142
PCI bus IF
141
140
ACK control section
142b
Address decoder
142a
Memory write control section
Data register
143
Address register
144
BE register
145
Memory
146

FIG. 18

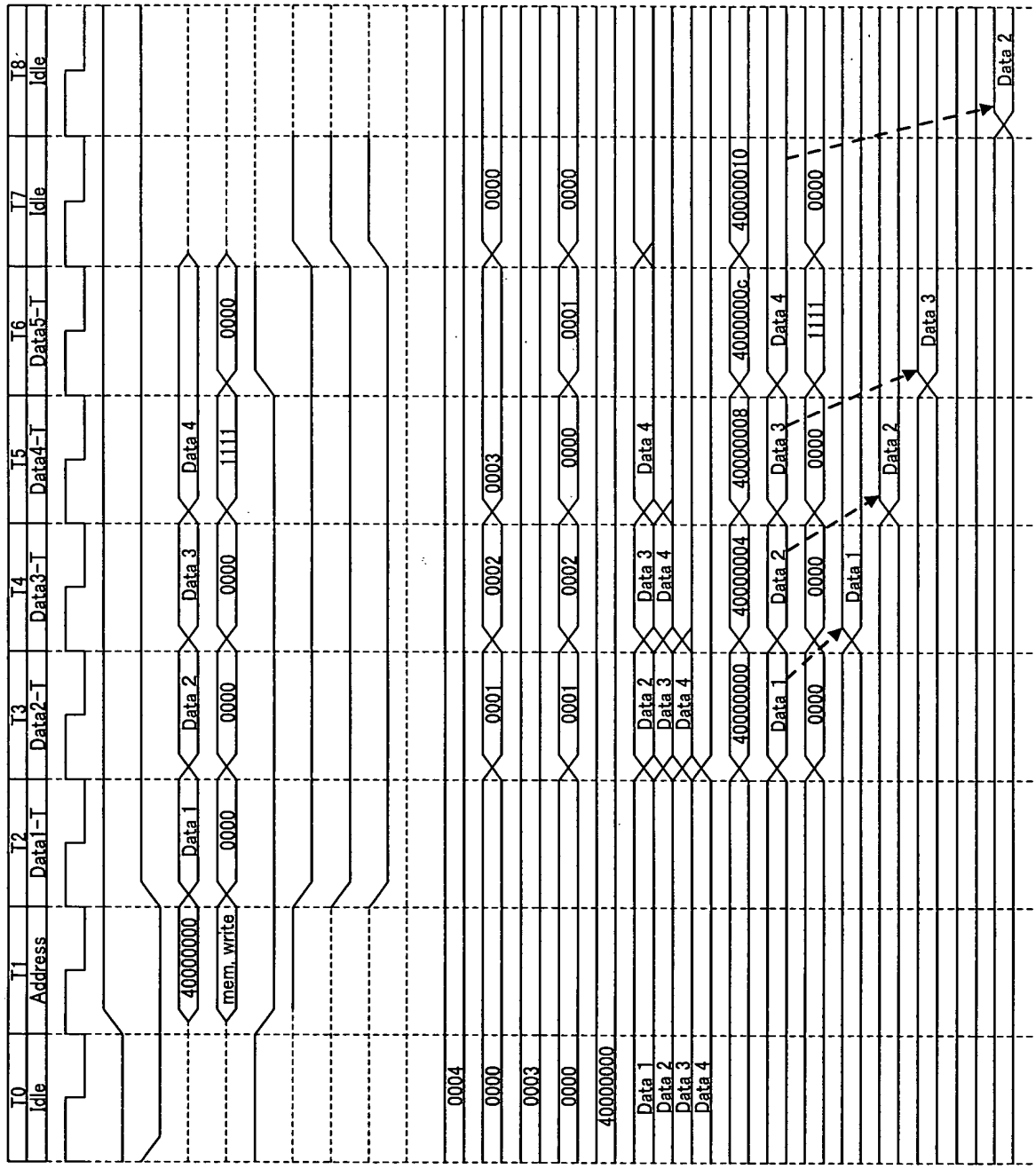

Time frame(300a)
Bus status(300c)
T0
Idle
T1
Address
T2
Data1-T
T3
Data2-T
T4
Data3-T
T5
Data4-T
T6
Data5-T
T7
Idle
T8
Idle
Clock(clk)(301a)
REQ#(301b)
GNT#(301c)
ad[31:0](302)
40000000
Data 1
Data 2
Data 3
Data 4
c_be#(303)
mem. write
0000
0000
0000
1111
0000
frame#(304)
irdy#(305)
trdy#(306)
devsel#(307)
stop#(321)
Transferred-word number register(308)
0004
Transferred-word number counter(309)
0000
0001
0002
0003
0000
Non-transfer interval register(1810)
0003
Non-transfer interval counter(1811)
0000
0001
0002
0000
0001
0000
Transfer destination start address register(312)
40000000
Data buffer(313)
a
b
c
d
Data 1
Data 2
Data 3
Data 4
Data 2
Data 3
Data 4
Data 3
Data 4
Address register(315)
40000000
40000004
40000008
4000000c
40000010
Data register(316)
Data 1
Data 2
Data 3
Data 4
Byte enable register(317)
0000
0000
0000
1111
0000
40000000th address(318)
Data 1
40000004th address(319)
Data 2
40000008th address(320)
Data 3
4000000cth address(328)
40000010th address(329)
Data 2

FIG. 19

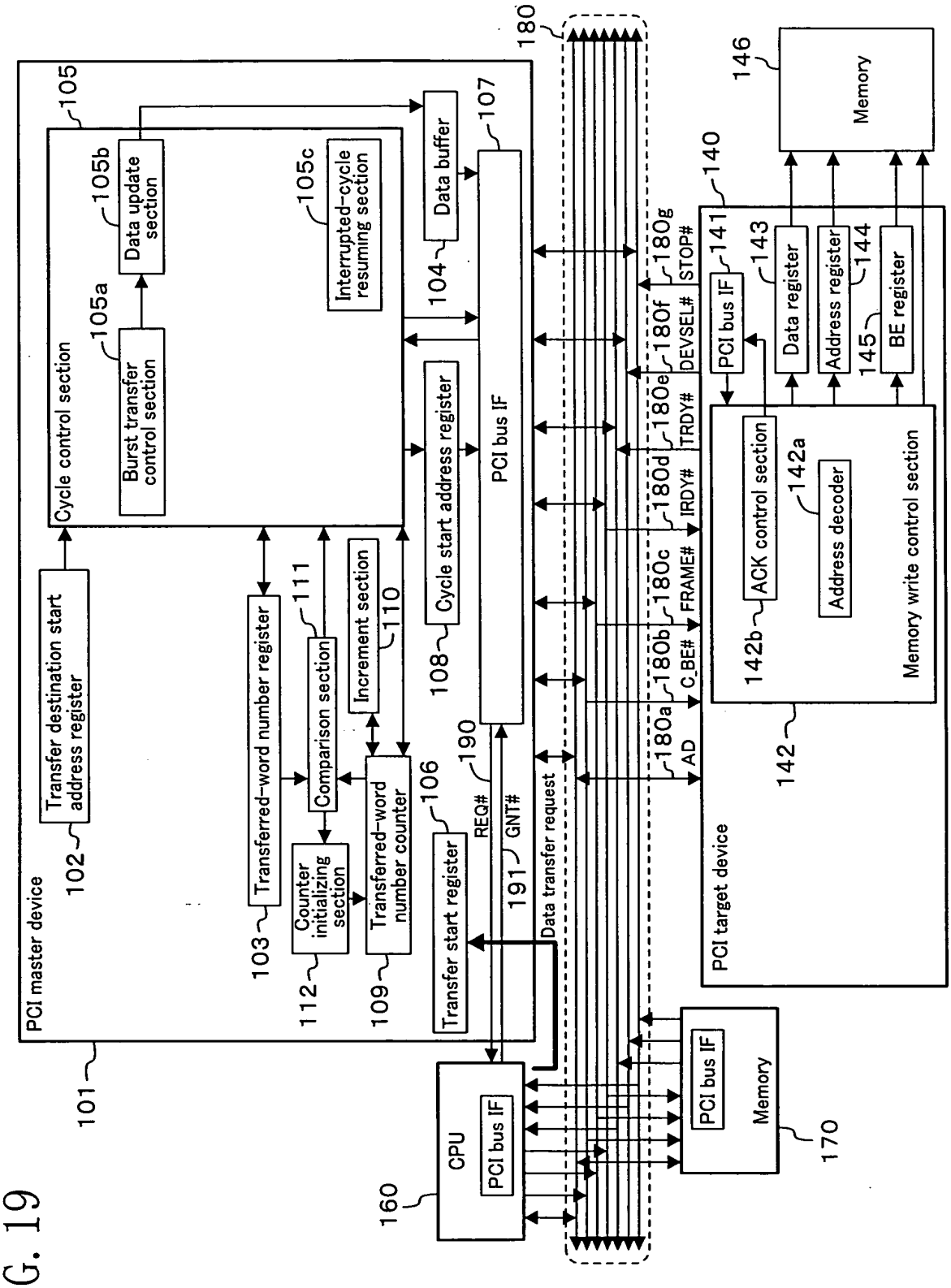

PCI master device
101
Cycle control section
105
Burst transfer control section
105a
Data update section
105b
Interrupted-cycle resuming section
105c
Transfer destination start address register
102
Transferred-word number register
103
Counter initializing section
112
Comparison section
111
Increment section
110
Transferred-word number counter
109
Transfer start register
106
Cycle start address register
108
Data buffer
107
PCI bus IF
104
180
REQ#
GNT#
190
191
Data transfer request
AD
C_BE#
FRAME#
IRDY#
TRDY#
DEVSEL#
STOP#
180a
180b
180c
180d
180e
180f
180g
CPU
PCI bus IF
160
Memory
PCI bus IF
170
PCI target device
142
PCI bus IF
141
ACK control section
142b
Address decoder
142a
Memory write control section
140
Data register
143
Address register
144
BE register
145
Memory
146

FIG. 20A

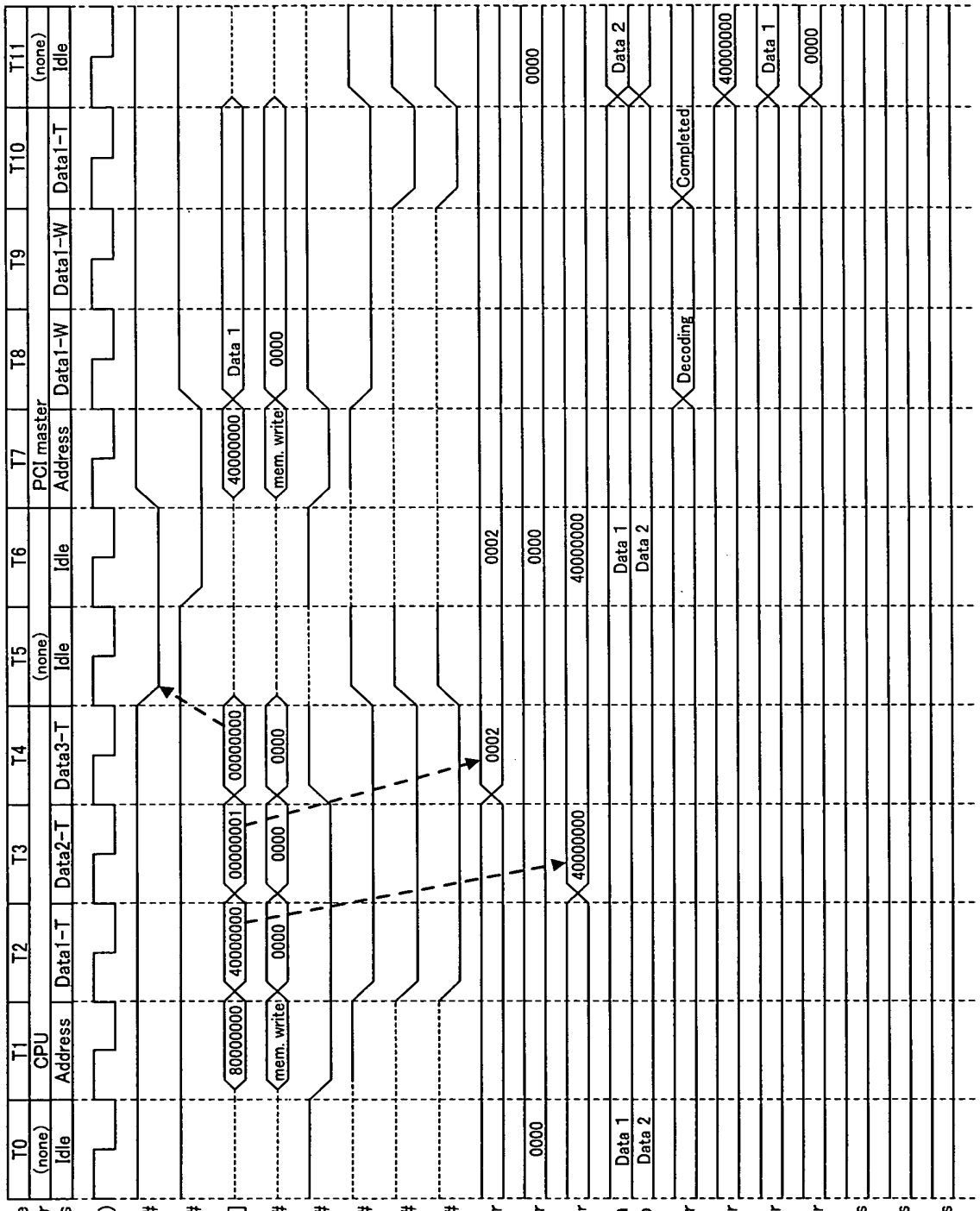
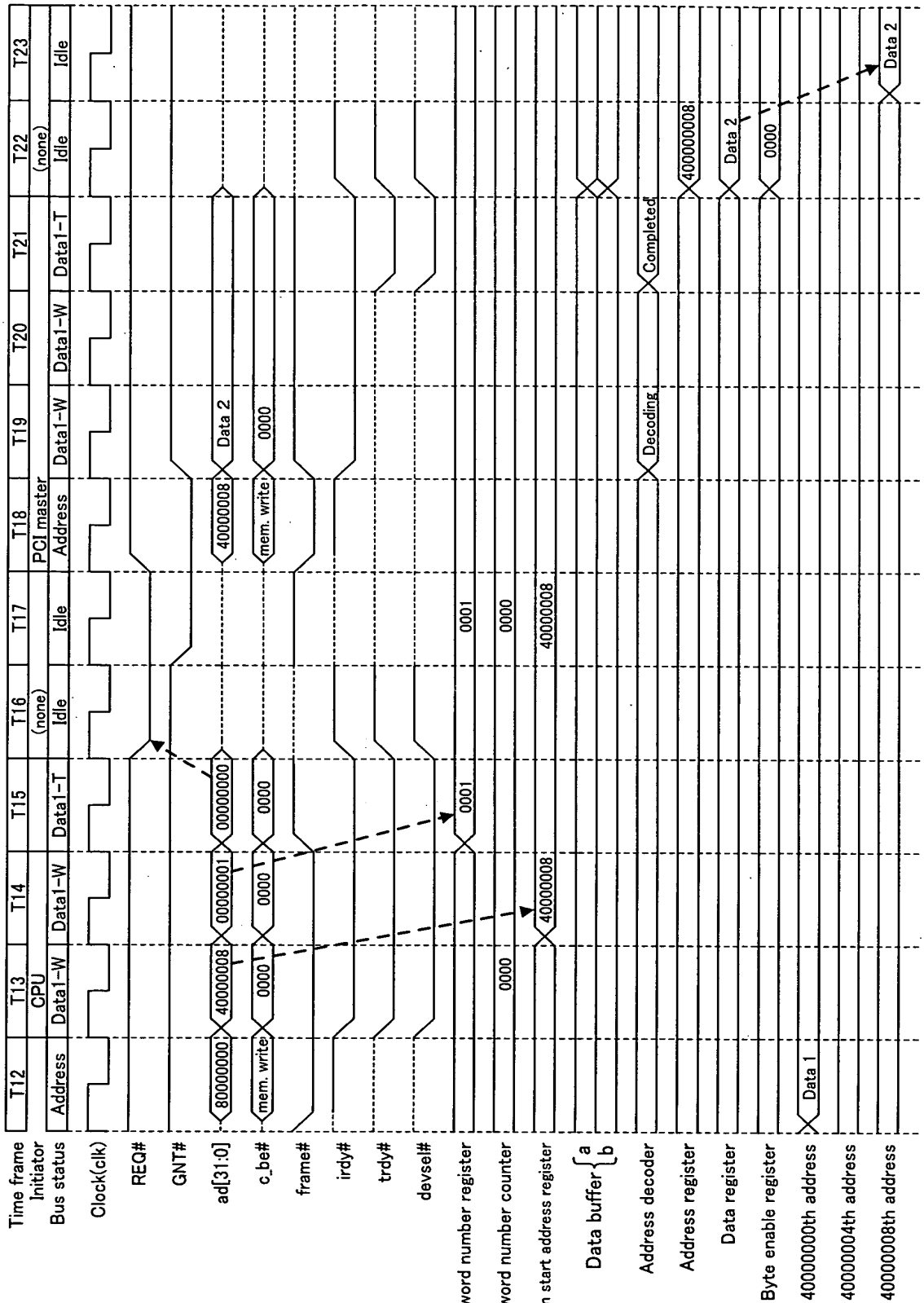

Setting of transfer to address 40000000 by CPU
Transfer to address 40000000
Time frame
Initiator
Bus status
Clock(clk)
REQ#
GNT#
ad[31:0]
c_be#
frame#
irdy#
trdy#
devsel#
Transferred-word number register
Transferred-word number counter
Transfer destination start address register
Data buffer
Address decoder
Address register
Data register
Byte enable register
40000000th address
40000004th address
40000008th address
T0 T1 T2 T3 T4 T5 T6 T7 T8 T9 T10 T11
(none) CPU (none) PCI master (none)
Idle Address Data1-T Data2-T Data3-T Idle Idle Address Data1-W Data1-W Data1-T Idle
80000000 40000000 00000001 00000000 40000000 Data 1
mem. write 0000 0000 0000 mem. write 0000
0000 0002 0002 0000 0000
40000000 40000000
Data 1 Data 2
Data 2 Data 1
Decoding Completed
40000000
Data 1
0000

FIG. 20B


Setting of transfer to address 40000008 by CPU
Transfer to address 40000008
Time frame
Initiator
Bus status
T12
T13
T14
T15
T16
T17
T18
T19
T20
T21
T22
T23
CPU
PCI master
(none)
(none)
Address
Data1-W
Data1-W
Data1-T
Idle
Idle
Address
Data1-W
Data1-W
Data1-T
Idle
Idle
Clock(clk)
REQ#
GNT#
ad[31:0]
80000000
40000008
00000001
00000000
40000008
Data 2
c_be#
mem. write
0000
0000
0000
mem. write
0000
frame#
irdy#
trdy#
devsel#
Transferred-word number register
0001
0001
Transferred-word number counter
0000
0000
Transfer destination start address register
40000008
40000008
Data buffer
a
b
Address decoder
Decoding
Completed
Address register
40000008
Data register
Data 2
Byte enable register
0000
40000000th address
Data 1
40000004th address
40000008th address
Data 2